CERN openlab III

Major Review
Platform CC

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Agenda

- Teaching
- Performance optimization
  - IPP performance optimizations in ROOT
- Multicore research
  - MT Geant4 on Dunnington and Nehalem
- Nehalem technical report
- Preliminary SSD evaluation
- Compiler comparisons using performance counters
- Conclusion

Teaching (1)
S. Jarp and A. Nowak

- 2 workshops held so far this year:
  - Computer Architecture and Performance Tuning: 12/13 March
    - Performance optimization; Computer architecture; Compilers
  - Multi-threading and Parallelism: 2/3 June
    - Multi and many-core technologies
    - Intel Threading Software tools discussed
  - Jeff Arnold from Intel's compiler group is now a regular teacher
  - High demand, good reviews: demand was so strong that additional exercise sessions had to be scheduled

- More workshops planned:
  - Computer Architecture and Performance Tuning: 6/7 October
  - Multi-threading and Parallelism: 18/19 November

Teaching (2)

- Teaching at the CERN School of Computing 2009 (Göttingen, Germany)
- Revised performance tuning program to be offered at the INFN computing school (Oct.)
- In addition: 1 workshop on “inside the core” optimization was held for expert CERN developers, with speakers from Intel
  - 20 participants from CERN
  - Centered on Intel’s Performance Tuning Utility (PTU) and advanced software optimization strategies
- Another Intel workshop planned, focused on multi-core optimization

Performance optimization (1)
A. Nowak

- New performance standard accepted in the Linux kernel – NOT perfmon2, that we are using
  - Perfmon2 will be supported and developed further in the future
  - Long term strategy not clear yet – new proposition is not mature enough to justify a switch
- Perfmon2 deployed in CERN's central software repository, now available for all standard managed nodes in the computing center
- Intel PTU being examined, looking forward to version 4.0
- New HP Nehalem systems arrived in the computing center
  - Same performance monitoring compatibility problems as with the previous batch (BIOS issue)

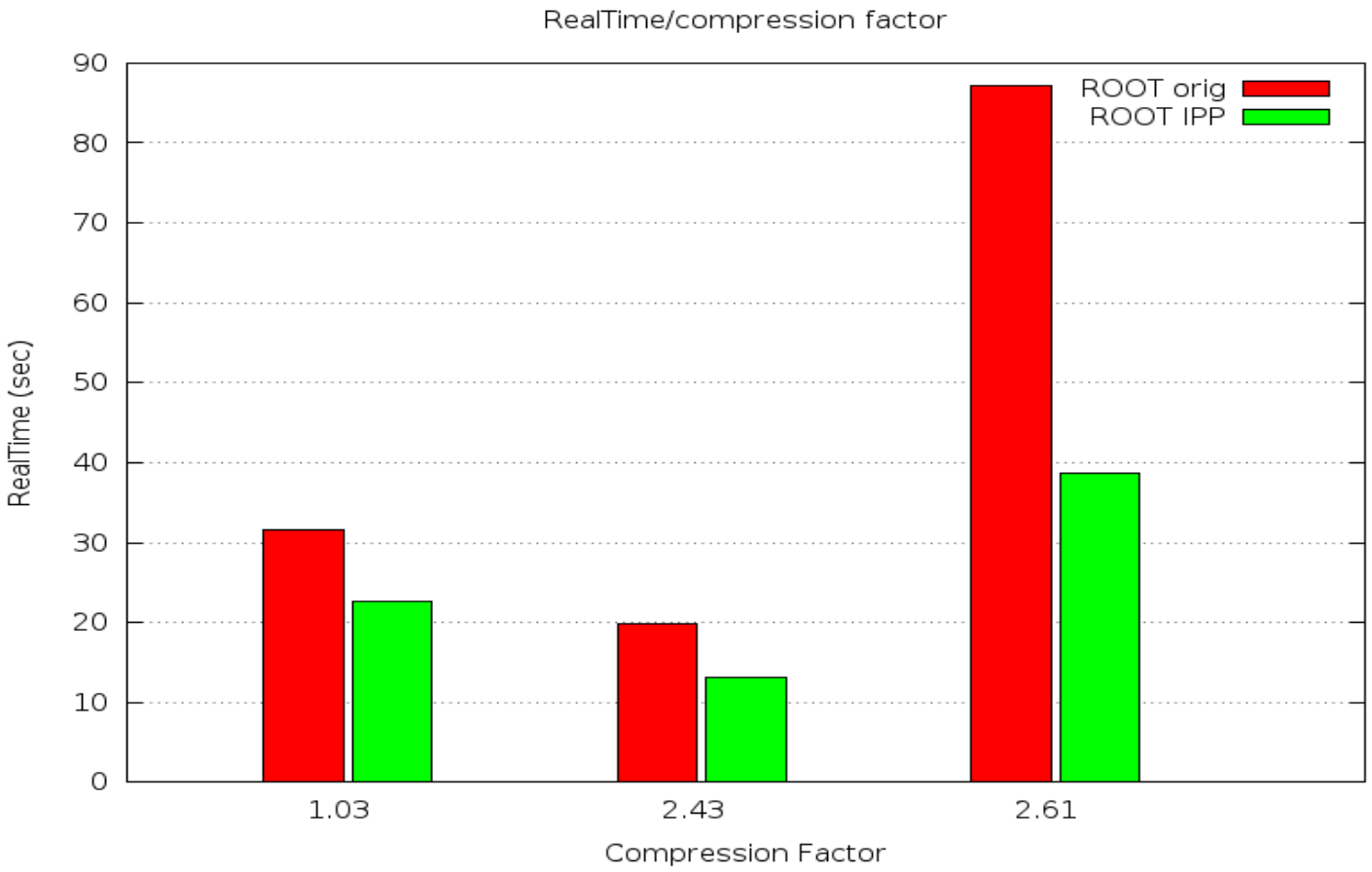
Performance optimization (2)

- Intel Integrated Performance Primitives examined
  - Work done by M. D'Arcy (summer student) – report published
  - IPP plugged into the ROOT framework to accelerate compression (up to 2.25x speedup reported)
- New Intel tools deployed centrally on AFS, available site-wide
  - Latest versions of the threading tools
  - Intel C++ and Fortran compilers 11 series
  - PTU 3.2.1

IPP compression optimizations in ROOT (M. D'Arcy)

Compression	CSize/OrigSize	Mbytes/sec	Throughput
IPP zlib	2.43 2.61	26.87 9.10	151% 225%
ROOT zlib	2.47 2.61	17.69 4.04	100% 100%

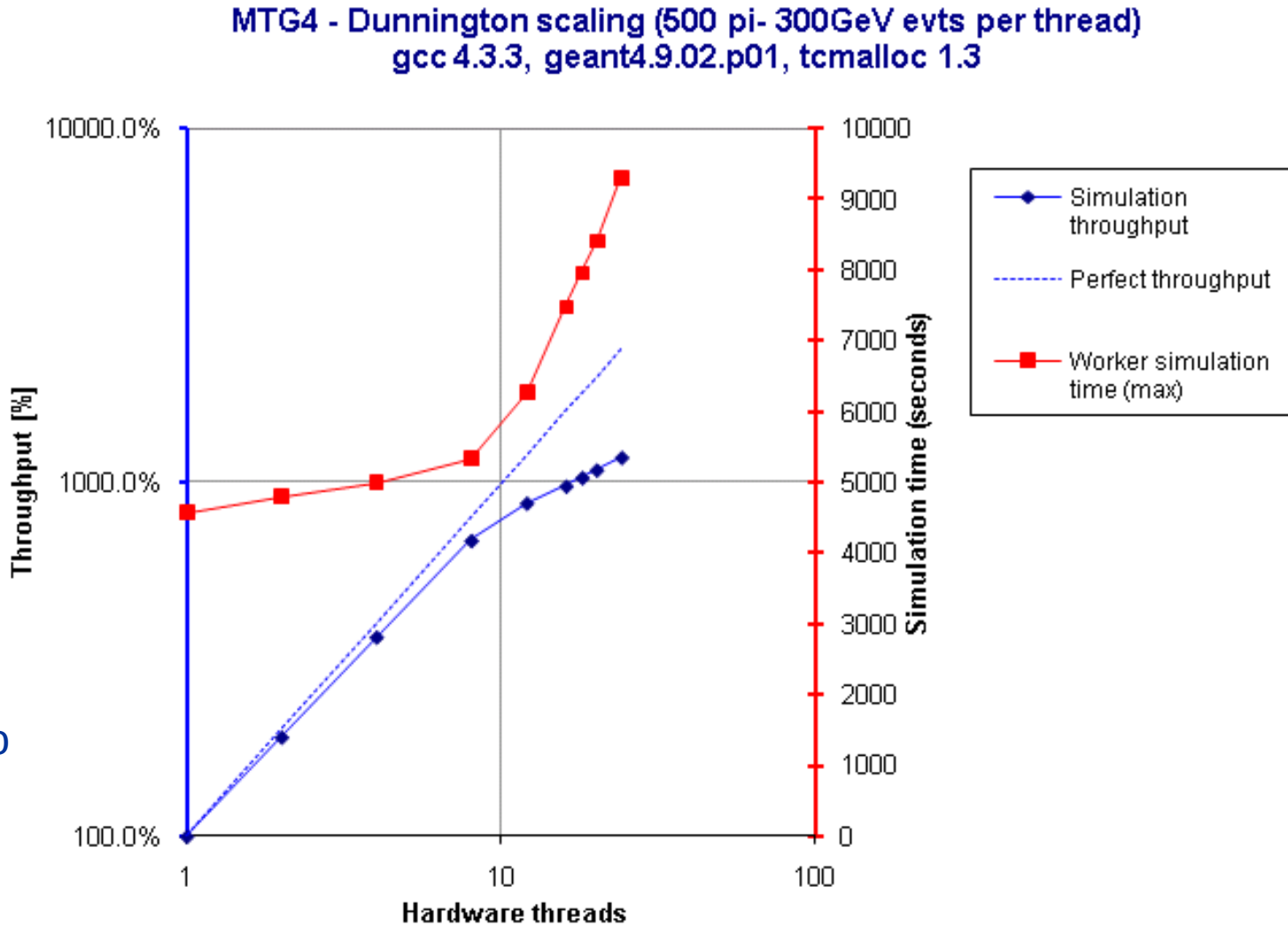
A 3rd compression algorithm was added, for IPP's zlib based compression



Multi-core research
A. Nowak

- Extensive testing of a multi-threaded Geant4 prototype on a 24-core Intel Xeon (Dunnington) based machine
  - Source code prepared by Xin Dong and Gene Cooperman from Northeastern University
  - Runs FullCMS Geant4 jobs with an arbitrary number of threads
  - First round of scalability and performance studies concluded, work continues
  - Valuable information gathered – both about the software and the hardware (Intel threading tools also used in the process)
  - Developed process and tools for future studies of this kind
- Performance analysis of a multi-threaded Geant4 prototype on Nehalem systems
  - Results in M. D'Arcy's report

MT Geant4 prototype loop fragment
Thread concurrency & efficiency

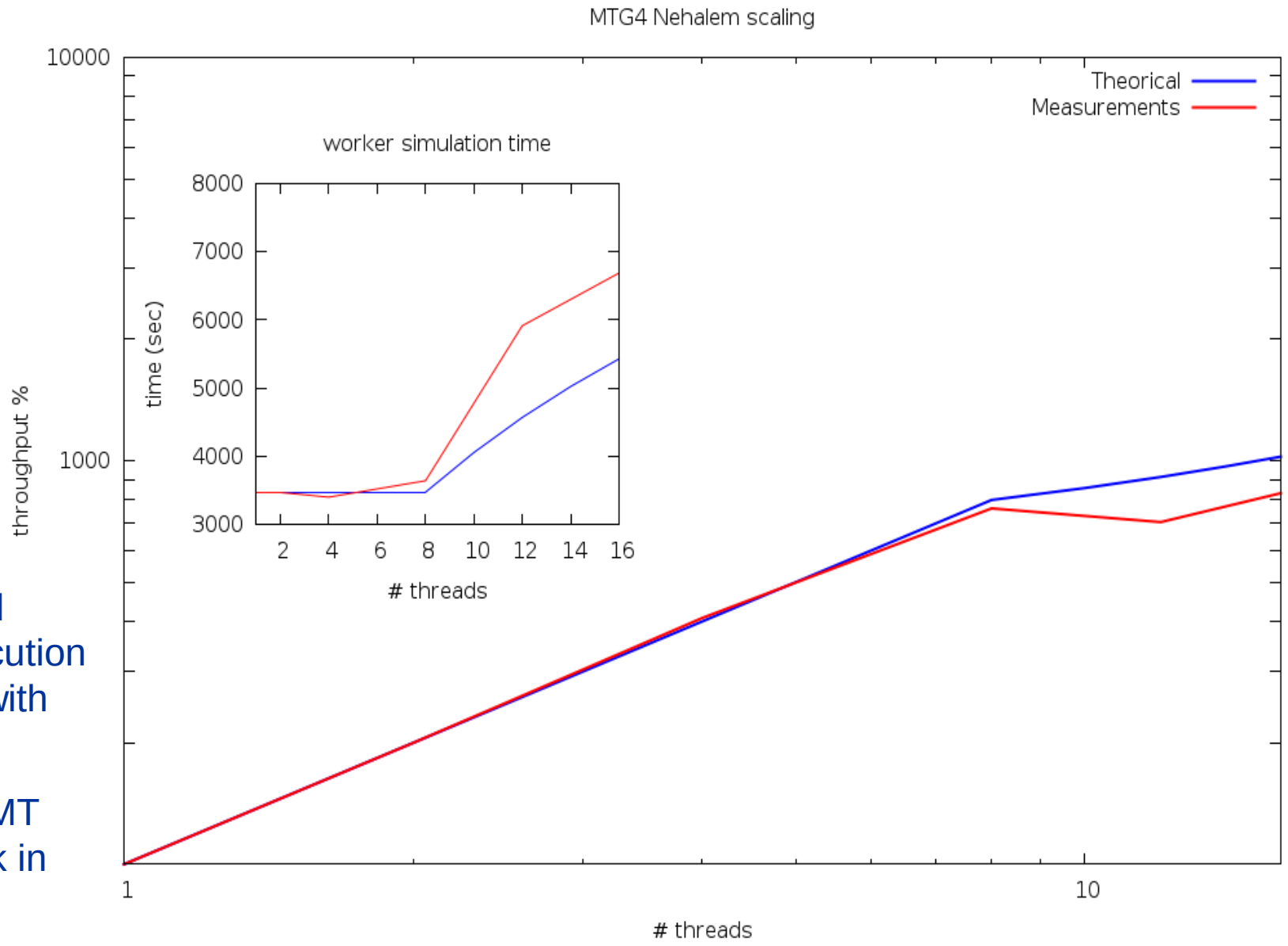


After updating malloc, other bottlenecks seem to prohibit scalability.

The red line should be flat!

MT Geant4 prototype scalability on Nehalem

M. D'Arcy



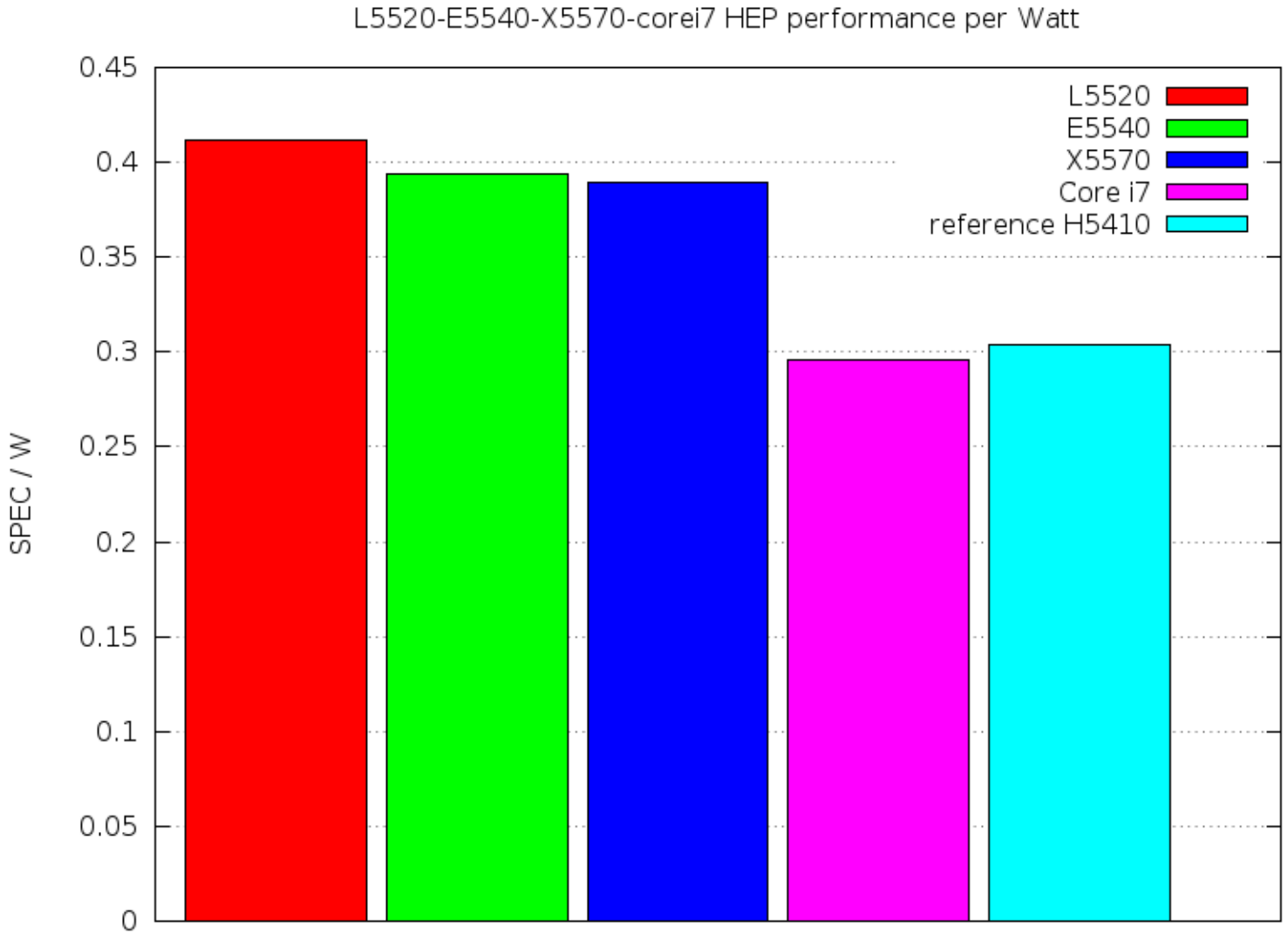
As expected shorter execution times than with Dunnington

>8 CPUs SMT starts to kick in

Nehalem Technical Report (1)

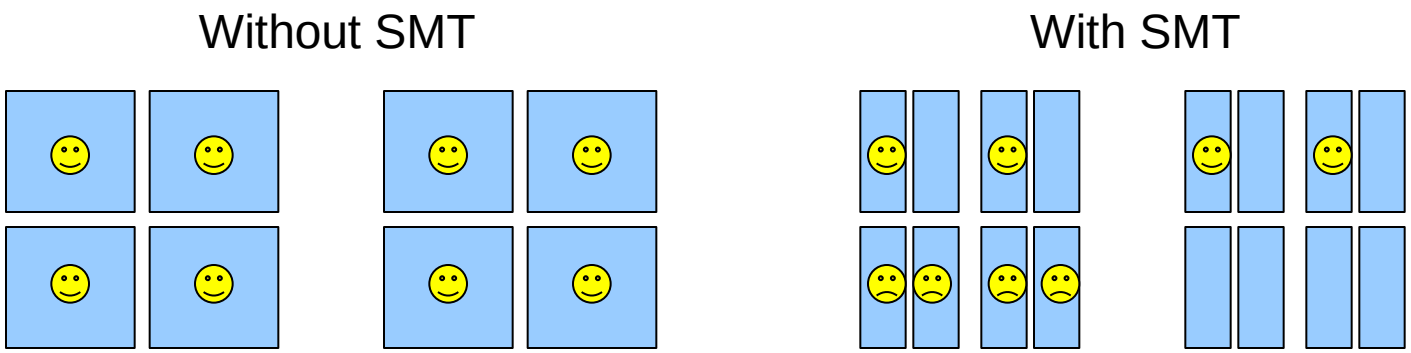
- Comprehensive technical report written by A. Busch (technical student) and J. Leduc
- Early Nehalem production-level server was used to evaluate the new Intel microarchitecture, and its new features
  - 3 CPU flavors evaluated: L5520, E5540, X5570
    - Benchmarks (SPEC2006, tbb, test40)
    - L5520 being the most efficient (36% more efficient than Harpertown using SPEC/W)
  - Turbo
  - The return of SMT (Simultaneous MultiThreading)

Nehalem Technical Report (2)

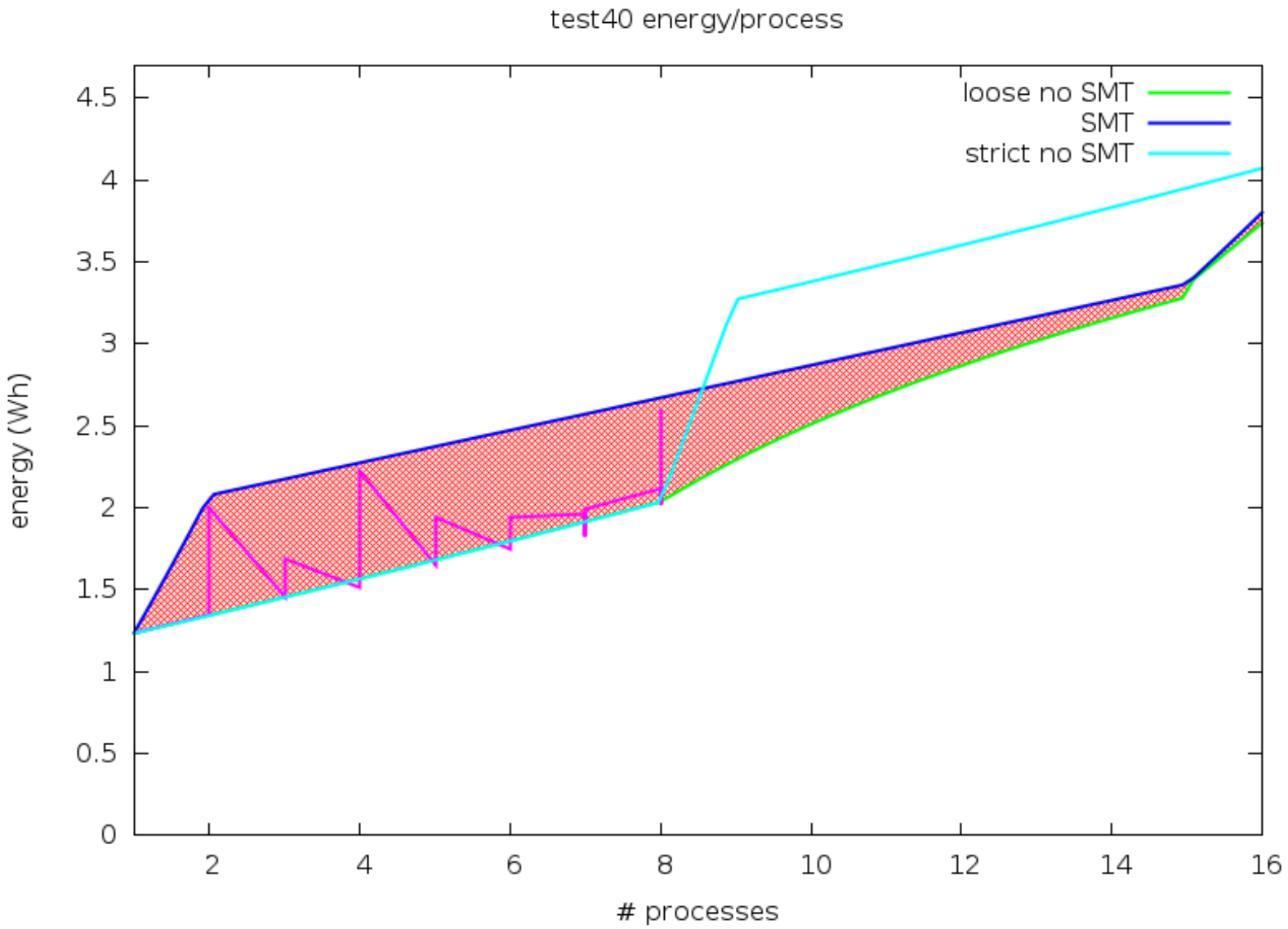


Nehalem Technical Report (3)

- SMT thoroughly evaluated
  - Observed a gain of throughput in the 15-21% range for all our tests (tbb, test40, hybrid tbb/test40 and Alice framework)
  - Old Irwindale server re-tested to validate initial implementation with current Linux kernel (SLC 5.3)
- The main initial performance problem (on Irwindale) came from OS schedulers limitations: they were not aware of the full CPU topology for SMT systems

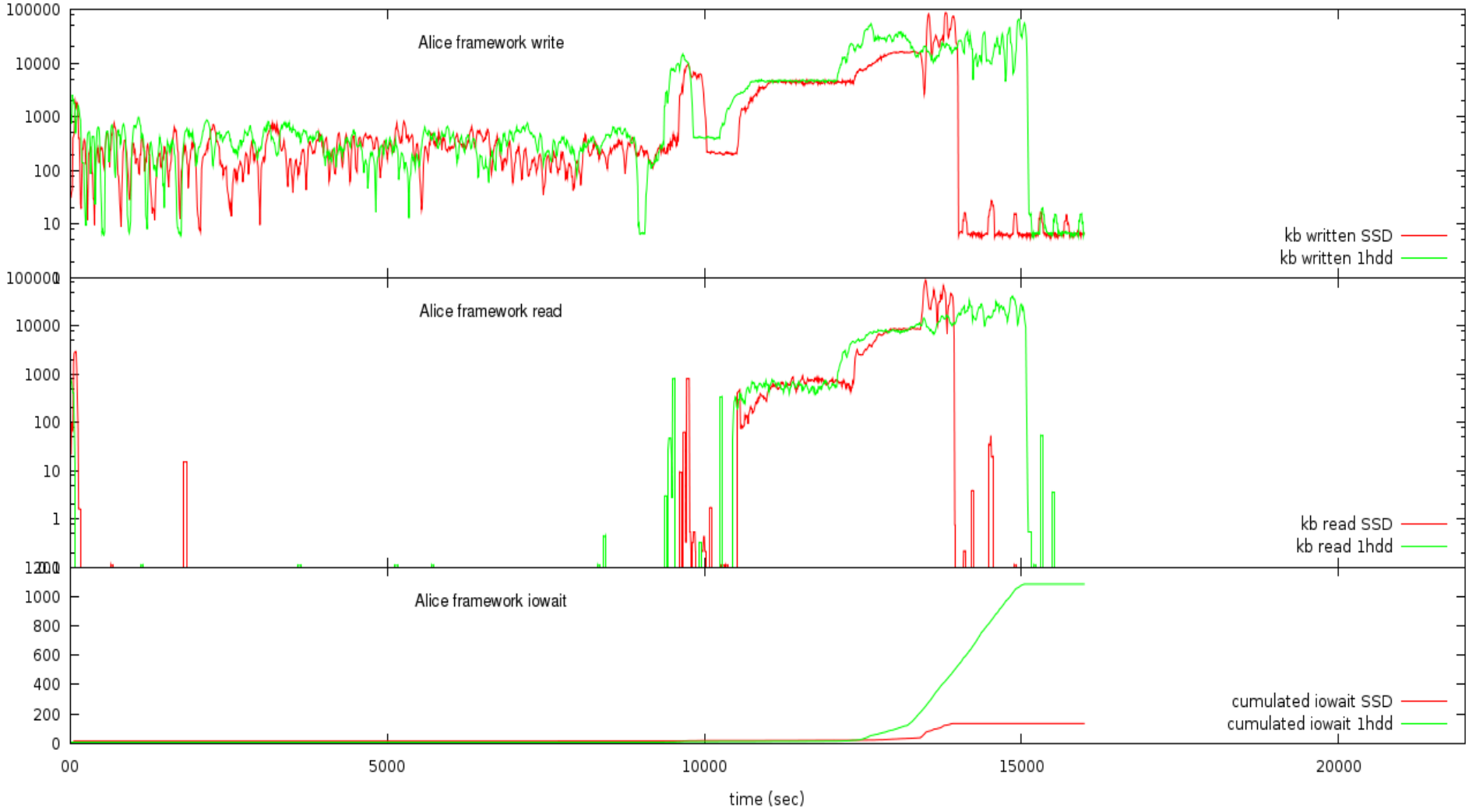


Nehalem Technical Report (4)



Preliminary SSD evaluation on Nehalem server

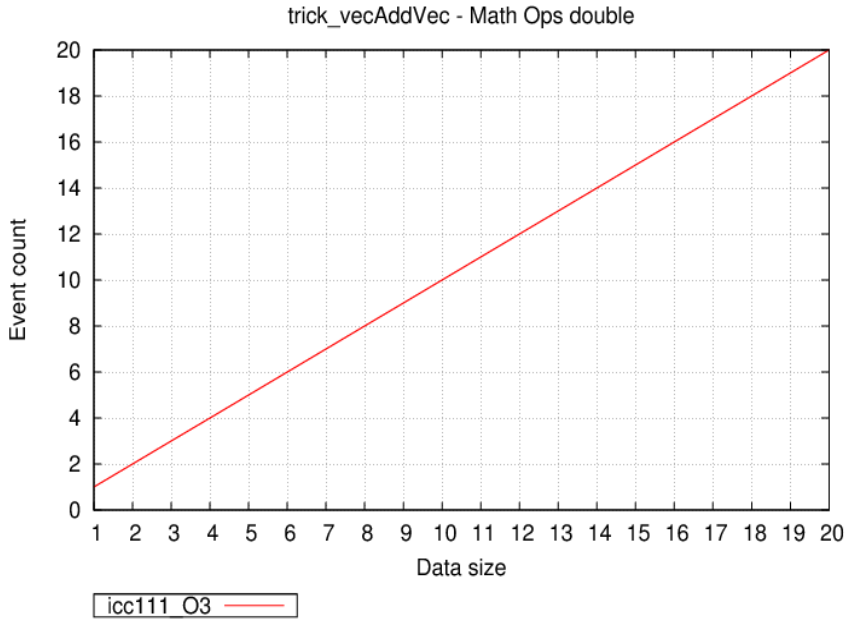
Evaluation of our engineering sample SSD: 32GB SLC SSD

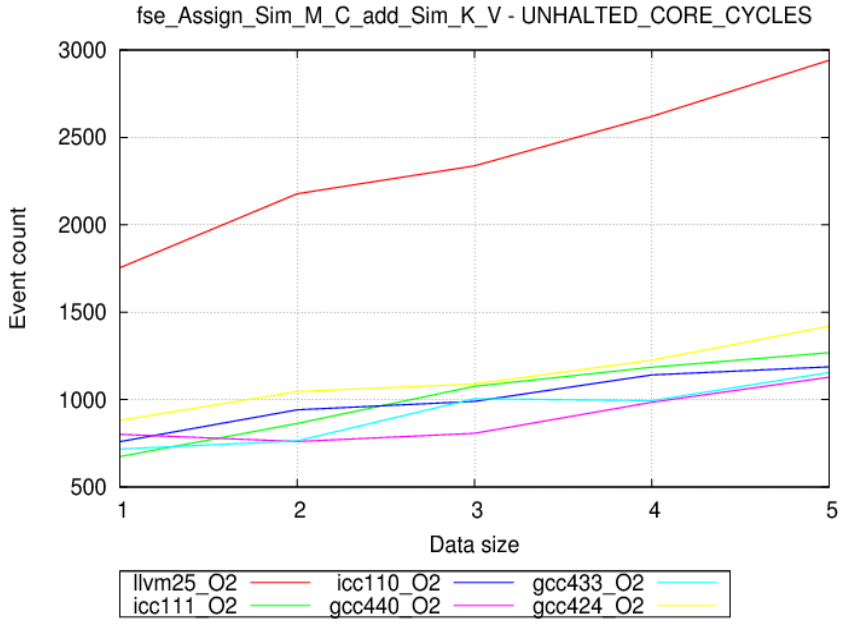


Compiler comparisons using performance counters (1)

- Extensive testing of different compilers on a set of benchmarks
  - Work done by R. Jensen (Summer Student)
  - 60 pages report (to be discussed with Intel)
- A framework was implemented to test various compilers and their options:
  - Standardized benchmark suite each:
    - Performing computations on data with variable size (vectors, matrices)
    - taking as an argument the number of iterations for the computational loop (the framework decides to run the loop for 100, 1000 or 10000 times)
  - Generates “off-line” graphs, with all the gathered statistics, according to a user query

Compiler comparisons using performance counters (2)





Scaling mathematical operations

Comparing various compilers on the same code

Much more has been achieved

- see full report

Conclusion

- Good progress in the area of teaching
- Several good results and new tools available for performance optimization
  - Including the comprehensive compiler study
- Comprehensive Nehalem technical report ready for publication
- Multicore research will continue
  - MT Geant4: expecting Nehalem EX
- Expecting other interesting hardware from Intel in the near future